TITLE AMENDMENT

~~SEMICONDUCTOR CHIP HAVING A SUPPORTING MEMBER, TAPE SUBSTRATE, SEMICONDUCTOR PACKAGE HAVING THE SEMICONDUCTOR CHIP AND THE TAPE SUBSTRATE, AND THE~~ METHOD OF MANUFACTURING ~~THE SAME~~ SEMICONDUCTOR CHIP HAVING SUPPORTING MEMBER AND SEMICONDCUTOR PACKAGE HAVING THE SEMICONDUCTOR CHIP

SPECIFICATION AMENDMENT

Paragraph beginning at page 1, line 6, has been amended as follows:

This application claims the priority benefit of Japanese Patent Application No. 2001-219182, filed July 19, 2001, the entire disclosure of which is incorporated herein by reference. This application is a division of applicant's application Serial No. 10/197,529, July 18, 2002.

Paragraph beginning at page 1, line 20, has been amended as follows:

Referring to Fig. 20, a semiconductor chip 1 of the related arts, which is used for a semiconductor package, includes ~~a single supporting member 4,~~ pads 2~~,~~ and bump electrodes 3, each of which is formed on one of the pads 2. The pads 2 are formed on a single surface of the semiconductor chip 1, and the pads 2 are electrically connected to circuits formed in the semiconductor chip 1. The pads 2 are disposed in an area 30 along the side of the semiconductor chip 1. Each of the bump electrodes 3 has a top surface 3a and a height. An area

of the top surface 3a of the bump electrode 3 is determined by assemble characteristics and a connecting resistance, and the height of the bump electrode 3 is determined by the reliability of the connection.

Paragraph beginning at page 4, line 17, has been amended as follows:

The objective is achieved by a semiconductor chip having a substrate including a main surface, the substrate including on the main surface a frame-shaped ~~flame-shaped~~ first area, which is along sides, and a second area encompassed by the first area, a pad formed in the first area, a bump electrode formed on the pad and at least one supporting member formed on the second area.

Paragraph beginning at page 4, line 22, has been amended as follows:

The objective is further achieved by a tape substrate having a tape

including a main surface, the tape including a frame-shaped ~~flame-shaped~~ first area on the main surface, and a second area encompassed by the first area, a land electrode formed in the first area, an I/O electrode formed in the first area, a wiring pattern formed in the first area, the wiring pattern connecting the land electrode to the I/O electrode, a resist pattern formed on the wiring patter, and at least one supporting member formed in the second area.

Paragraph beginning at page 5, line 12, has been amended as follows:

The objective is achieved by a method of manufacturing a semiconductor chip having providing a substrate having a main surface, the substrate including on the main surface a frame-shaped ~~flame-shaped~~ first area, which is along sides, and a second area encompassed by the first area, forming a pad in the first area, forming a bump electrode on the pad, and forming at least one supporting member on the second area.

Paragraph beginning at page 8, line 11, has been amended as follows:

Referring to Fig. 1, a semiconductor chip 100 includes a single cylinder-shaped supporting member 4, pads 2, and bump electrodes 3, each of which is formed on one of the pads 2. The pads 2 are formed on a single surface of the semiconductor chip 1, and the pads 2 are electrically connected to circuits formed in the semiconductor chip 1. The pads 2 are disposed in a frame-shaped ~~flame-shaped~~ area 30 along the sides of the semiconductor chip 1. Each of the bump electrodes 3 has a top surface 3a and a height. An area of the top surface 3a of the bump electrode 3 is determined by the assemble characteristics and the connecting resistance, and the height of each bump electrode 3 is determined by the reliability of the connection. The supporting member 4 is formed on the same surface where the bump electrodes 3 are formed. In Fig. 1, since the bump electrodes are formed at regular intervals, the support member 4 may be located anywhere in an area 50, which is encompassed by the area 30, preferably at the center of the area 50. However, if the bump electrodes 3 are formed at irregular intervals, the support member 4

is preferably located at a certain station, which is spaced from each bump electrode 3 equally, or its vicinity. In this embodiment, although only the single support member 4 is formed, a plurality of support members may be formed in the area 50. Further, although the support member 4 is cylinder-shaped in this embodiment, the support member 4 can be formed in any shape. As described above, although the number and the shape of the support member can be changed, the number and the shape should be designed in consideration for a total area where the support members are formed and the total area where the support members are occupied within the area 50. If the support members are formed with high density or the occupancy rate of the support members in the area 50 is high, the flow of resin material, which is introduced later, is interfered by the support members.

Paragraph beginning at page 17, line 12, has been amended as follows:

Referring to Figs. 9 and 10, a tape substrate 400 includes land electrodes 6 to be connected to bump electrodes of semiconductor chip, I/O lead electrodes 14, wiring patterns 13, each of which connects ~~is connected~~ one of

the land electrodes 6 to one of the I/O lead electrodes 14, a single resist-formed supporting member 4b and a frame-shaped ~~flame-shaped~~ resist film 10. The surface of each land electrode 6 may be metal plated. The land electrodes 6, the I/O lead electrodes 14, the wiring patterns 13, the resist film 10 and the single resist-formed supporting member 4b are formed on the same surface of the tape substrate 400.

Paragraph beginning at page 18, line 8, has been amended as follows:

Comparing to the fourth embodiment, a supporting member 4 having two layers is formed in the fifth embodiment. Referring to Figs. 11 and 12, the tape substrate 500 includes land electrodes 6 to be connected to bump electrodes of the semiconductor chip, I/O lead electrodes 14, wiring patterns 13, each of which is connected one of the land electrodes 6 to one of the I/O lead electrodes 14, a single first supporting member 4b, a single second supporting member 4c and a frame-shaped ~~flame-shaped~~ resist film 10. The surface of the land electrode 6 may be metal plated. The land electrodes 6, the I/O lead electrodes 14, the wiring patterns 13, the resist film 10 and the first and second

supporting members 4b, 4c are formed on the same surface of the tape substrate 500. The second supporting member 4c is formed in an area, which is encompassed by the land electrode 6, the first supporting member 4b is formed on the second supporting member 4c.